

# 22320

11920

**3 Hours / 70 Marks**

Seat No.

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- Instructions* –
- (1) All Questions are *Compulsory*.
  - (2) Answer each next main Question on a new page.
  - (3) Illustrate your answers with neat sketches wherever necessary.
  - (4) Figures to the right indicate full marks.
  - (5) Assume suitable data, if necessary.
  - (6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

**Marks**

- 1. Attempt any FIVE of the following: 10**
- a) Convert  $(D8F)_{16}$  into binary and octal.
  - b) Draw Symbol, Truth Table and logic equation of Ex-OR gate.
  - c) State the DeMorgan's Theorems.
  - d) Convert the following expression into standard SOP form.  
$$Y = AB + \overline{AC} + BC$$
  - e) Draw symbol and write truth table of D and T Flip Flop.
  - f) Write down number of flip flops are required to count 16 clock pulses.
  - g) List the types of DAC

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- 2. Attempt any THREE of the following:** **12**
- a) Perform the subtraction using 2'S Complement methods.  
 $(52)_{10} - (65)_{10}$
- b) Simplify the following Boolean Expression and Implement using logic gate.  
 $ABC\bar{D} + AB\bar{C}D + ABCD + ABCD$
- c) Minimize the four variable logic function using K map.  
 $f(A,B,C,D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$
- d) Implement the following functions using demultiplexer.  
 $f_1 = \sum m(0, 2, 4, 6)$   
 $f_2 = \sum m(1, 3, 5)$
- 3. Attempt any THREE of the following:** **12**
- a) Realize the following logic expressions using only NAND gates.  
 (i) OR  
 (ii) AND  
 (iii) NOT
- b) Draw binary to gray converter and write its truth table.
- c) Describe the working of JK flip flop with truth table and logic diagram.
- d) Describe the working of 4 bit SISO (serial in serial out) Shift Register with diagram and waveform if input is 01101.
- 4. Attempt any THREE of the following:** **12**
- a) Design a full Adder using Truth Table and K-map.
- b) Describe the working of ring counter using D flip flop with diagram and waveforms.
- c) Draw block diagram of programmable logic Array.
- d) Compare the following:  
 (i) Volatile with Non Volatile.  
 (ii) EPROM with EEPROM.
- e) Describe the working principle of successive approximation ADC.

**5. Attempt any TWO of the following:**

- a) (i) Convert the following binary number  $(11001101)_2$  into Gray Code and Excess-3 Code.
- (ii) Perform the BCD Addition.  
 $(17)_{10} + (57)_{10}$
- (iii) Perform the binary addition.  
 $(10110 \cdot 110)_2 + (1001 \cdot 10)_2$
- b) Design a 4bit ripple counter using JK flip flop, with truth table and waveforms.
- c) Calculate the analog output for 4 bit weighted register type DAC for inputs
- (i) 1011
- (ii) 1001
- Assume  $(V_{fs})$  full scale range of voltage is 5V

**6. Attempt any TWO of the following:****12**

- a) Compare TTL, CMOS and ECL logic family on the following points.
- (i) Basic Gates
- (ii) Propagation delay
- (iii) Fan out
- (iv) Power Dissipation
- (v) Noise immunity
- (vi) Speed Power Product.
- b) Design a BCD adder using IC 7483.
- c) Design a 3 bit synchronous counter using JK FlipFlop.
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